

FIG. IA (PRIOR ART)

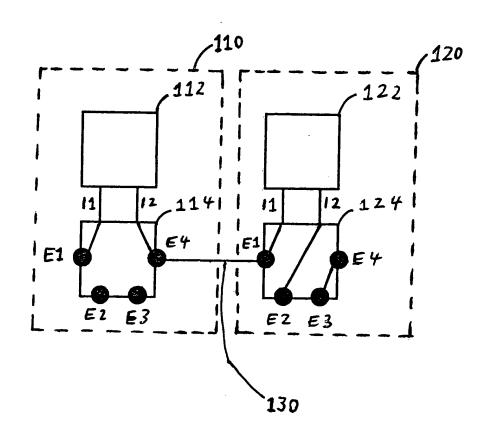


FIG. 1B (PRIOR ART)

(1,4)	(2,4)	(3,4)	(4,4)	(5,4)

$$(1,1)$$
 $(2,1)$ $(3,1)$ $(4,1)$ $(5,1)$

FIG. 1 (PRIOR ART)

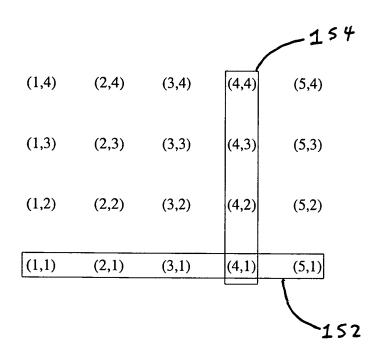


FIG. 1D (PRIOR ART)

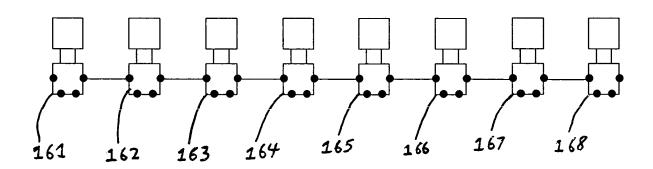


FIG. 1E (PRIOR ART)

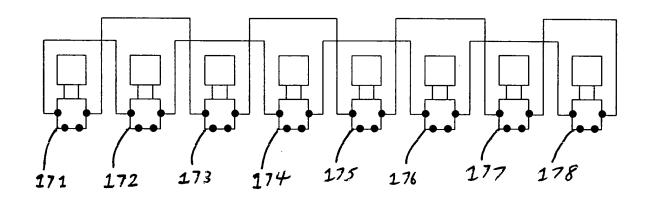


FIG. 1F (PRIOR ART)

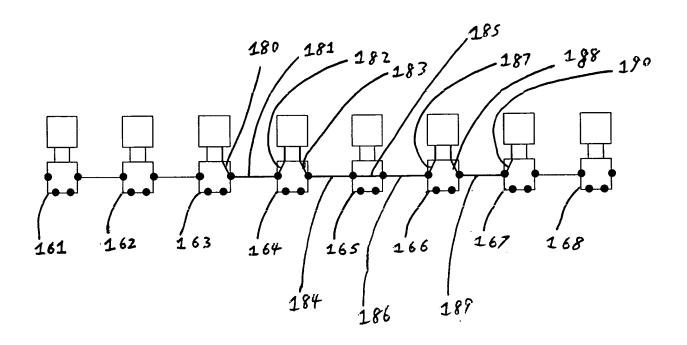
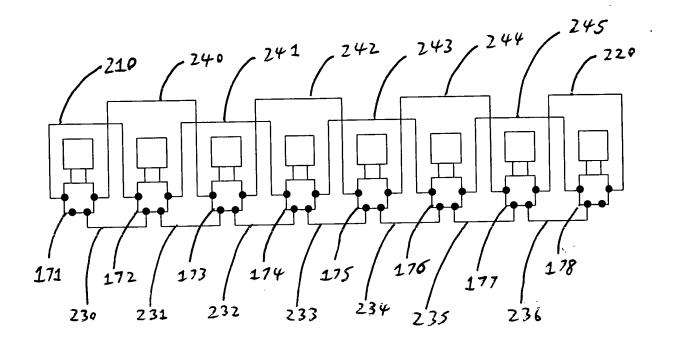
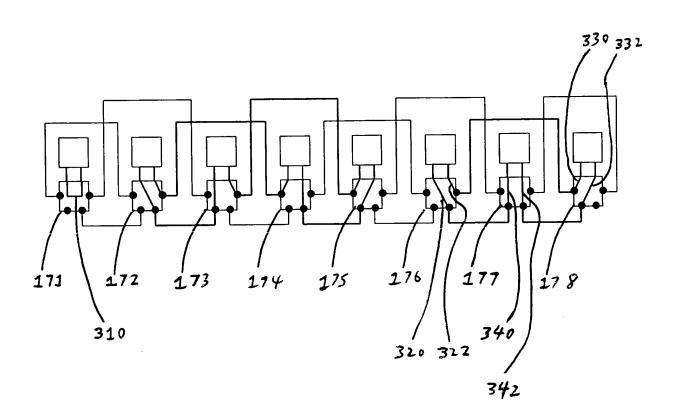
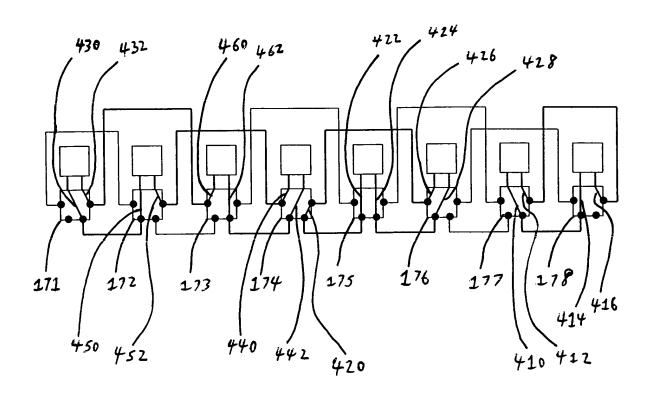


FIG. 1G (PRIOR ART)

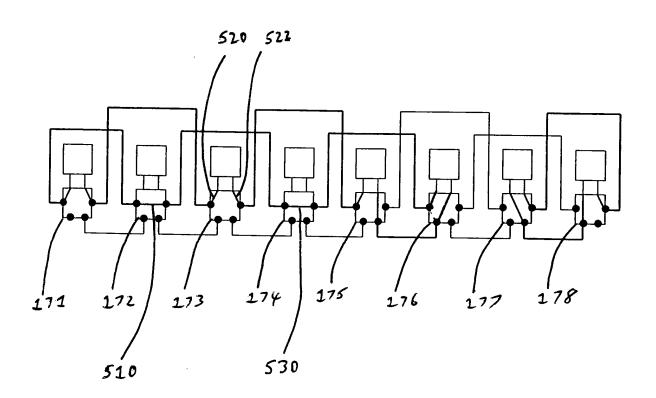


F16.2





F16.4



F16,5

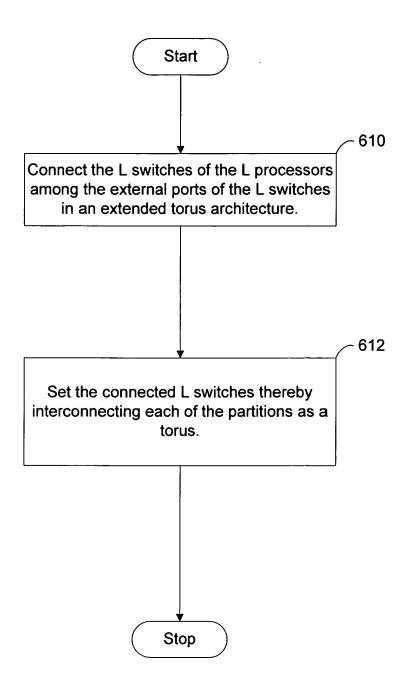


FIG. 6

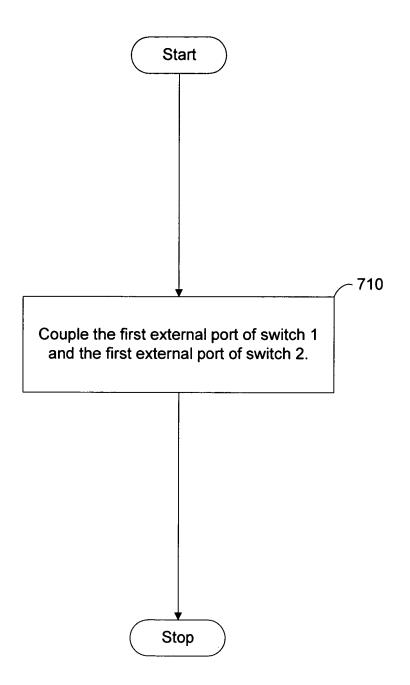
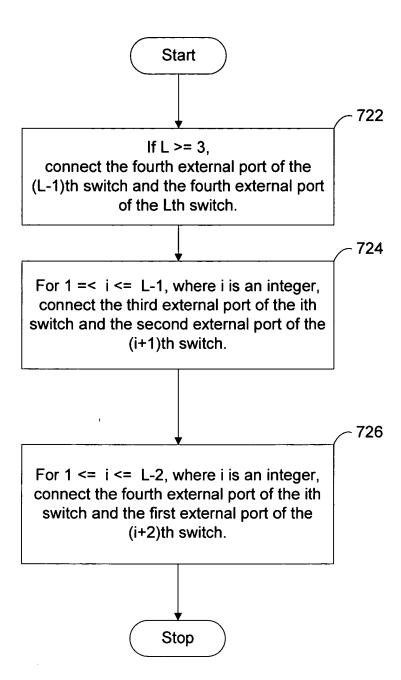


FIG. 7A



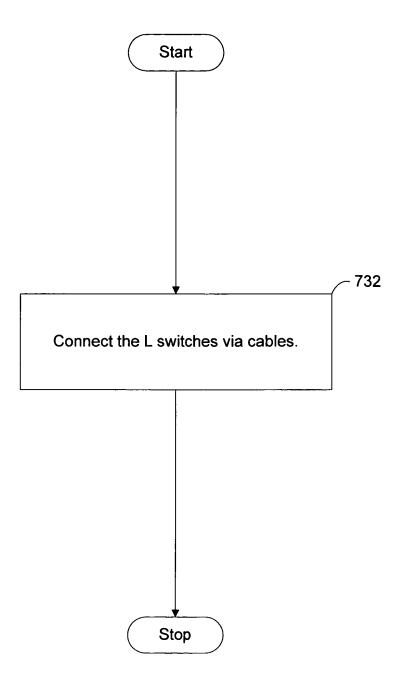


FIG. 7C



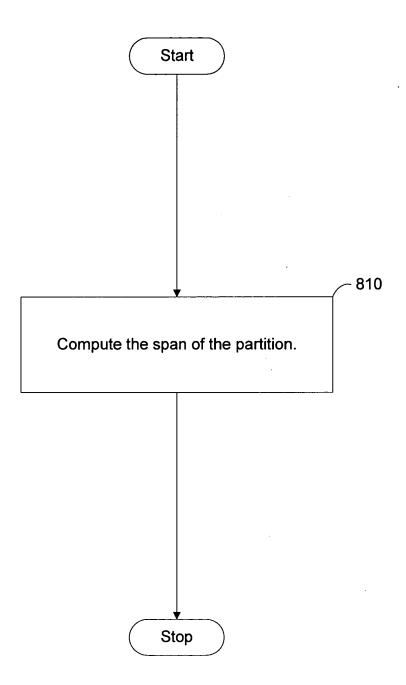


FIG. 8A

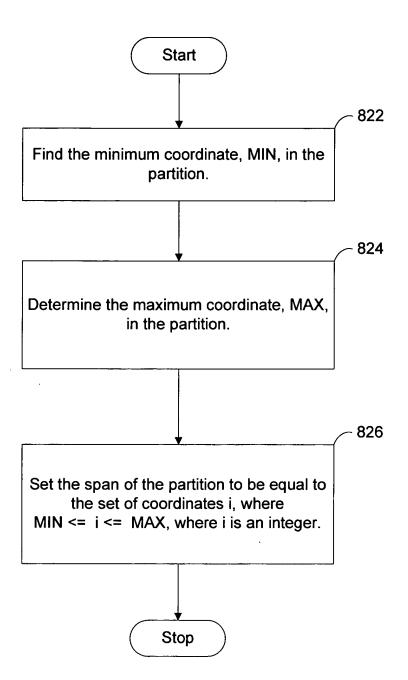


FIG. 8B



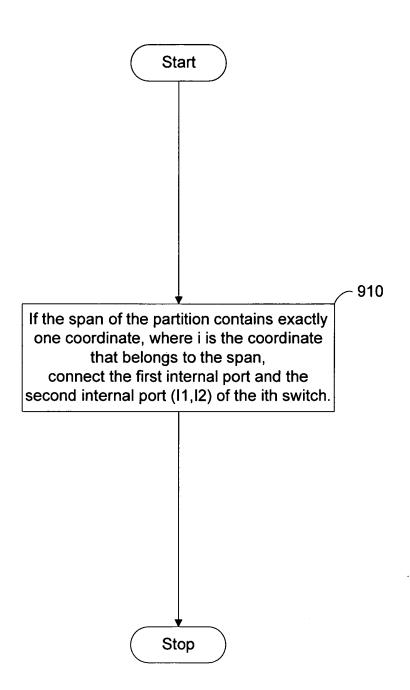


FIG. 9



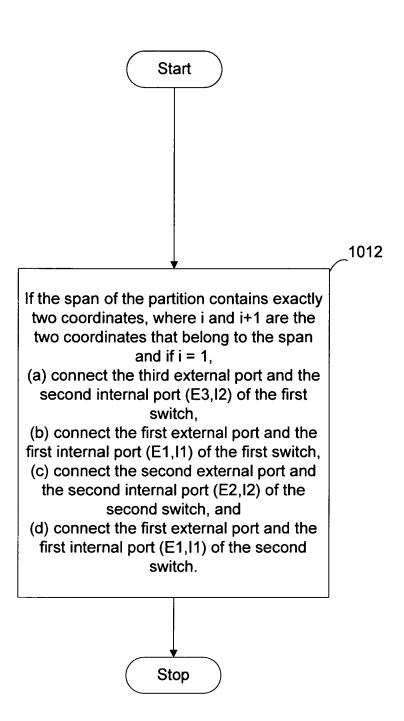


FIG. 10A



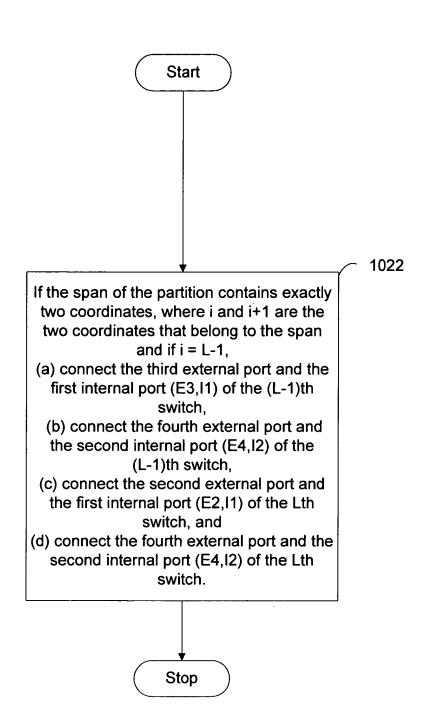
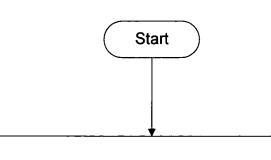


FIG. 10B



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If the span of the partition contains exactly two coordinates, where i and i+1 are the two coordinates that belong to the span and otherwise, where

$$2 \le i \le L-2$$
,

- (a) connect the third external port and the fourth external port (E3,E4) of the (i-1)th switch,
- (b) connect the second external port and the first internal port (E2,I1) of the ith switch,
- (c) connect the third external port and the second internal port (E3,I2) of the ith switch,
- (d) connect the first external port and the first internal port (E1,I1) of the (i+1)th switch, and
- (e) connect the second external port and the second internal port (E2,I2) of the (i+1)th switch.

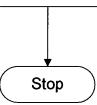


FIG. 10C

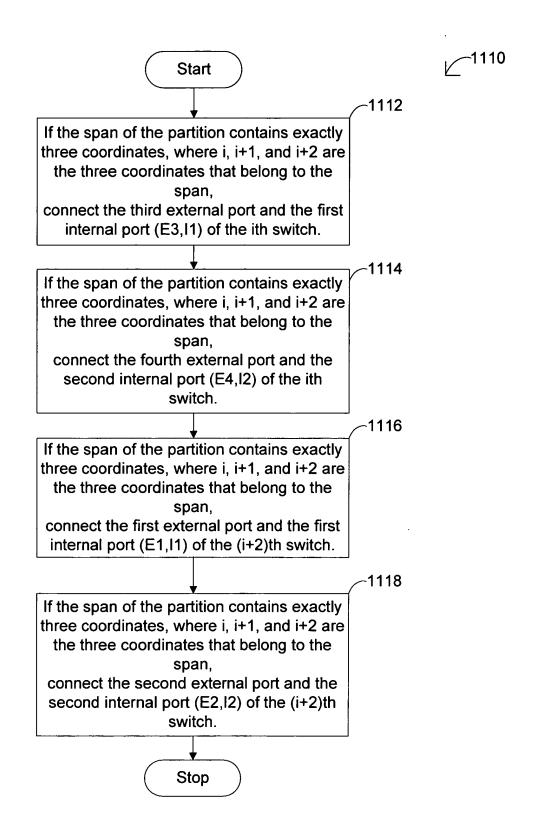


FIG. 11A

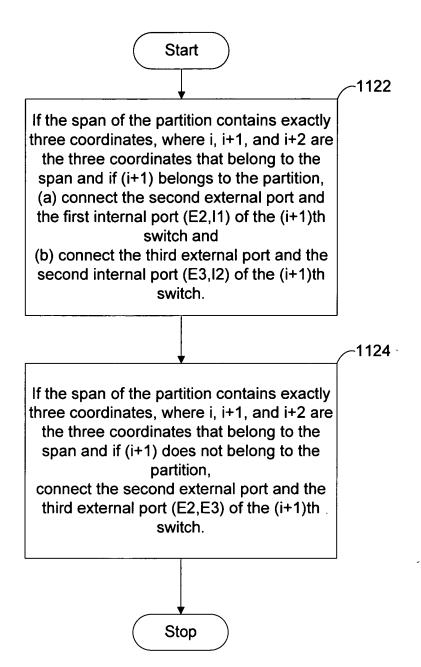


FIG. 11B



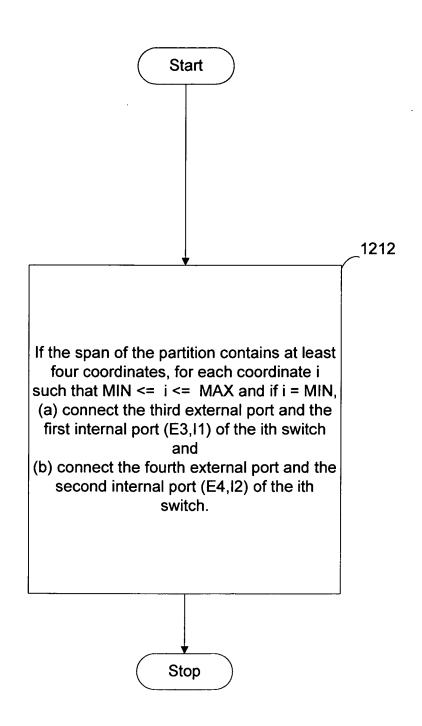


FIG. 12A



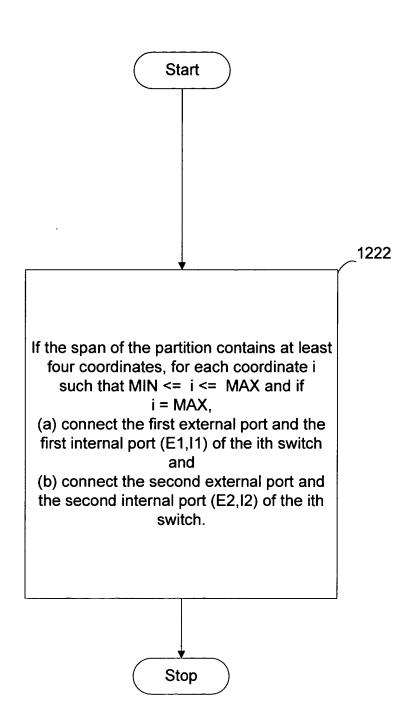


FIG. 12B



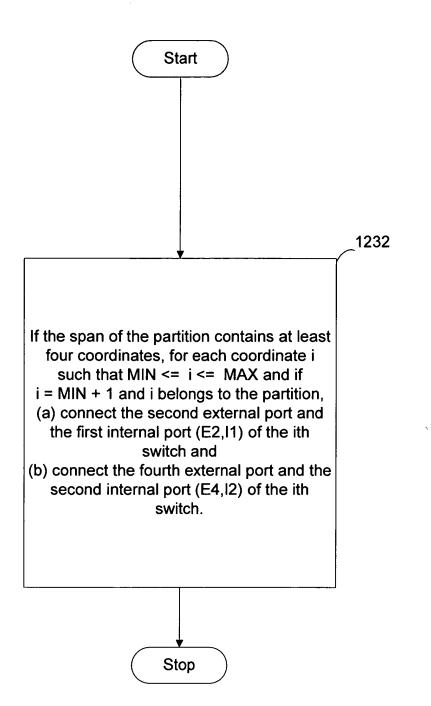


FIG. 12C



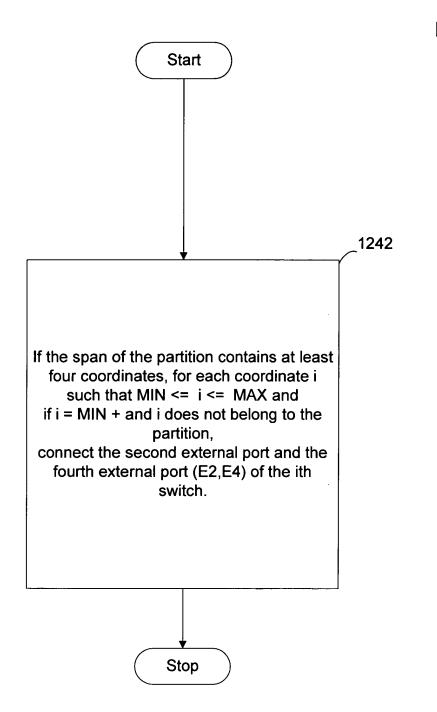


FIG. 12D



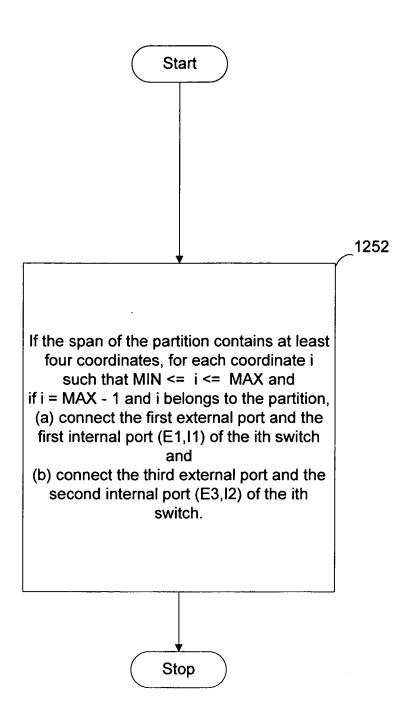


FIG. 12E



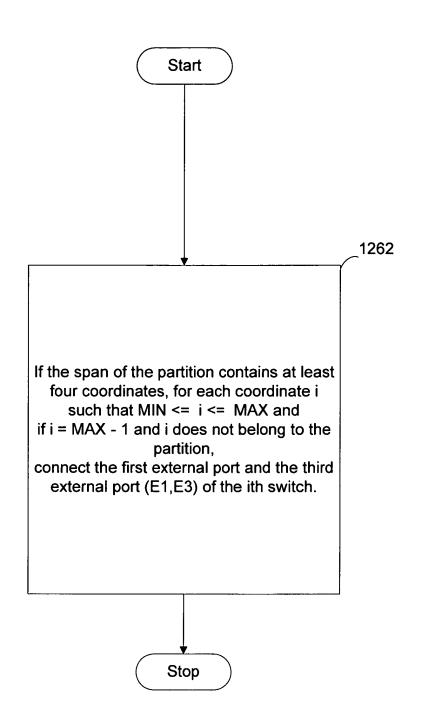


FIG. 12F



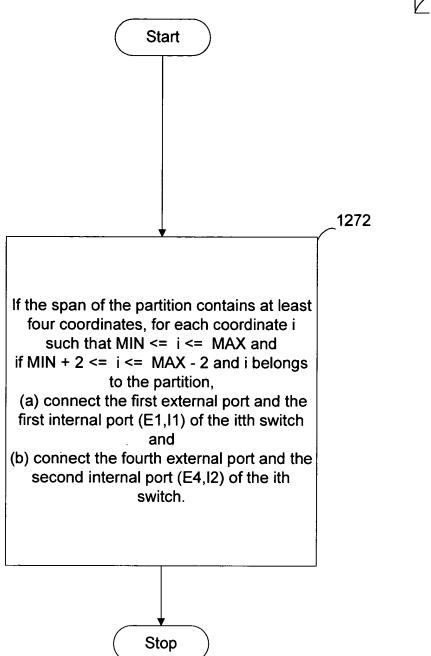


FIG. 12G



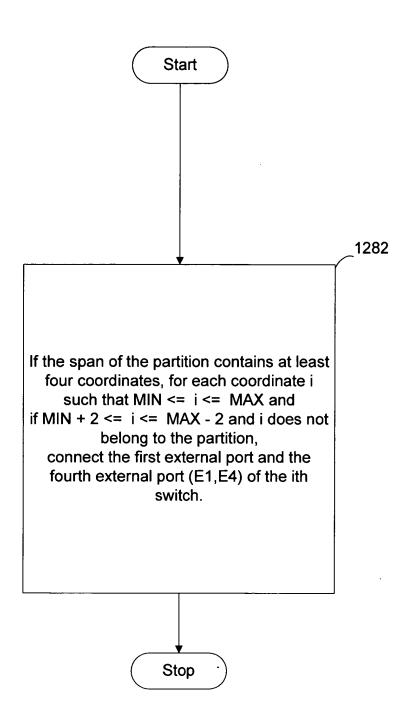


FIG. 12H

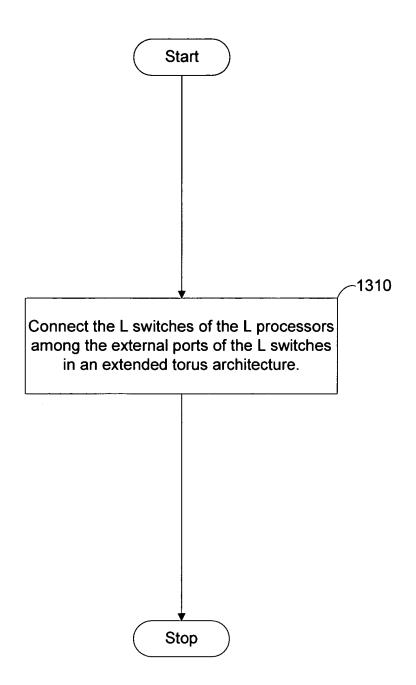


FIG. 13A



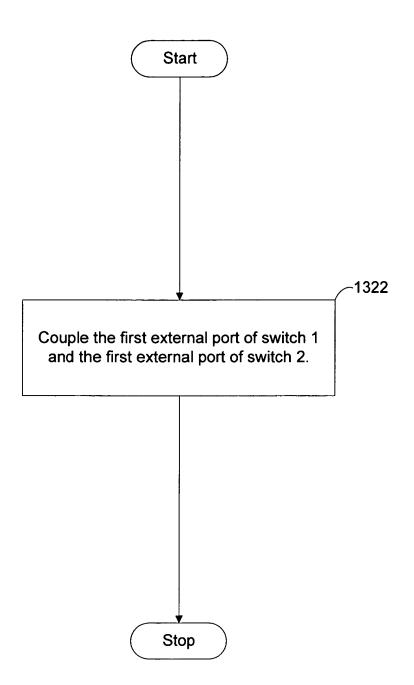


FIG. 13B

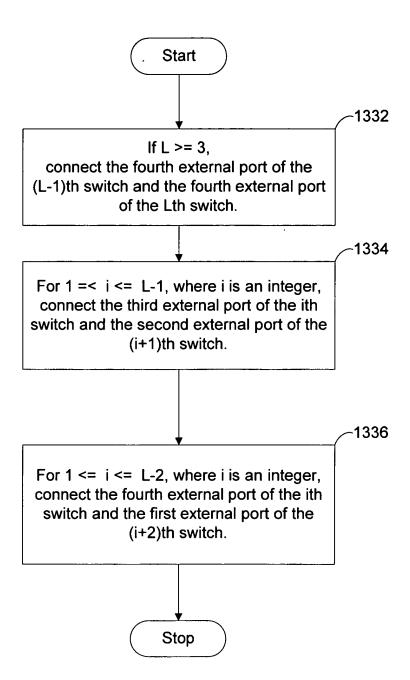


FIG. 13C

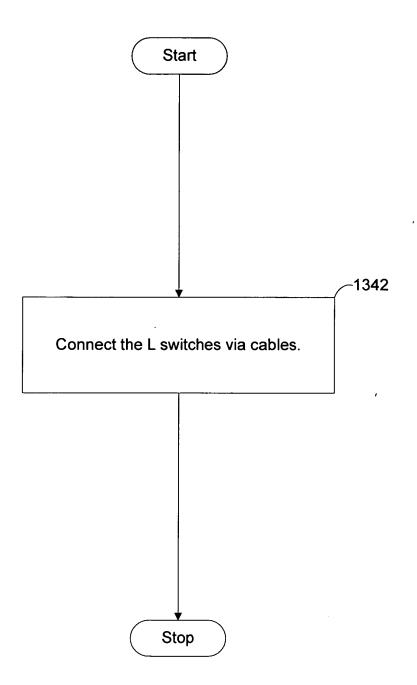


FIG. 13D

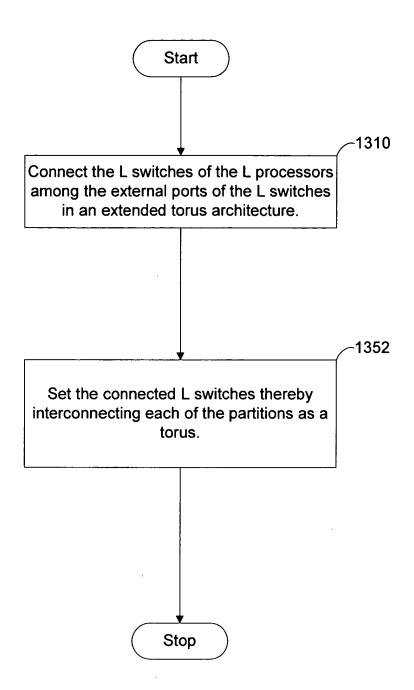


FIG. 13E

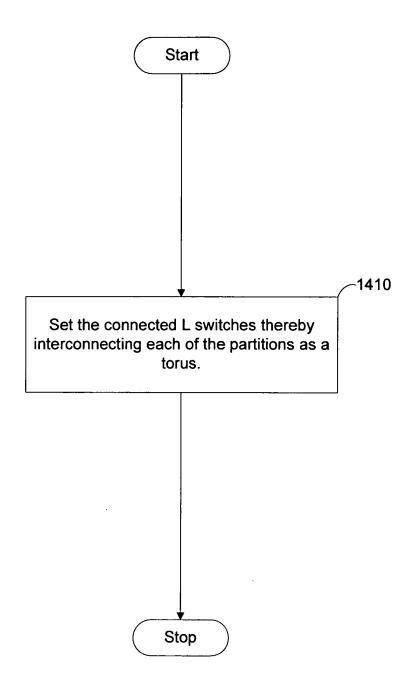


FIG. 14